

CLAIMS

WHAT IS CLAIMED:

1. A dual mode built-in self-test controller, comprising:
a logic built-in self-test domain, including:
a logic built-in self-test engine capable of executing a logic built-in self-test;
and
a logic built-in self-test signature generated by an execution of the logic built-in self-test; and
a memory built-in self-test domain, including:
a memory built-in self-test engine capable of executing a memory built-in self-test.
2. The dual mode built-in self-test controller of claim 1, wherein the logic built-in self-test engine comprises:
a logic built-in self-test state machine; and
a pattern generator capable of generating a scan pattern for use in a state of the logic built-in self-test state machine.
3. The dual mode built-in self-test controller of claim 2, wherein the logic built-in self-test state machine further comprises:
a reset state entered upon receipt of an external reset signal;
an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;
a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;
a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and
a done state entered into from the step state when the content of the pattern generator equals the predetermined vector count.
4. The dual mode built-in self-test controller of claim 2, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

1 5. The dual mode built-in self-test controller of claim 2, wherein the logic built-
2 in self-test signature includes at least one of:

3 a bit indicating an error condition arose; and

4 a bit indicating whether the stored results are from a previous logic built-in self-test
5 run.

1 6. The dual mode built-in self-test controller of claim 1, wherein the memory
2 built-in self-test domain further comprises a memory built-in self-test signature generated by
3 an execution of the memory built-in self-test.

1 7. The dual mode built-in self-test controller of claim 6, wherein the memory
2 built-in self-test signature includes the results of at least one paranoid check.

1 8. The dual mode built-in self-test controller of claim 6, wherein the memory
2 built-in self-test signature includes a bit indicating whether a memory built-in self-test is
3 done.

1 9. The dual mode built-in self-test controller of claim 1, wherein the memory
2 built-in self-test engine comprises:

3 a memory built-in self-test state machine; and

4 a nested memory built-in self-test engine operating the memory built-in self-test state
5 machine.

1 10. The dual mode built-in self-test controller of claim 9, wherein the memory
2 built-in self-test state machine comprises

3 a reset state entered upon receipt of an external reset signal;

4 an initiate state entered from the reset state upon receipt of at least one of a memory
5 built-in self-test run signal and a memory built-in self-test select signal;

6 a flush state entered from the initiate state upon the initialization of components and
7 signals in the memory built-in self-test domain in the initiate state;

8 a test state entered into from the flush state upon completing a flush of a plurality of
9 memory components to a known state; and

10 a done state entered into upon completing the test of each of the memory components
11 in the memory built-in self-test.

1 11. The dual mode built-in self-test controller of claim 1, wherein the memory
2 built-in self-test engine comprises:

- 3 a plurality of alternative memory built-in self-test state machines; and
4 a nested memory built-in self-test engine operating a predetermined one of the
5 memory built-in self-test state machines.

1 12. The dual mode built-in self-test controller of claim 11, wherein each of the
2 memory built-in self-test engines comprises:

- 3 a reset state entered upon receipt of an external reset signal;
4 an initiate state entered from the reset state upon receipt of at least one of a memory
5 built-in self-test run signal and a memory built-in self-test select signal;
6 a flush state entered from the initiate state upon the initialization of components and
7 signals in the memory built-in self-test domain in the initiate state;
8 a test state entered into from the flush state upon completing a flush of a plurality of
9 memory components to a known state; and
10 a done state entered into upon completing the test of each of the memory components
11 in the memory built-in self-test.

1 13. A dual mode built-in self-test controller, comprising:

- 2 a logic built-in self-test domain, including:
3 means for executing a logic built-in self-test; and
4 means for storing the results of a logic built-in self-test generated by an
5 execution of the logic built-in self-test; and
6 a memory built-in self-test domain, including:
7 means for executing a memory built-in self-test.

1 14. The dual mode built-in self-test controller of claim 13, wherein the logic
2 executing means comprises:

- 3 a logic built-in self-test state machine; and
4 a pattern generator capable of generating a scan pattern for use in a state of the logic
5 built-in self-test state machine.

1 15. The dual mode built-in self-test controller of claim 13, wherein the memory
2 built-in self-test domain further comprises a means for storing the results of a memory built-
3 in self-test by an execution of the memory built-in self-test.

1 16. The dual mode built-in self-test controller of claim 13, wherein the memory
2 executing means comprises:

- 3 a memory built-in self-test state machine; and
4 a nested memory built-in self-test engine operating the memory built-in self-test state
5 machine.

1 17. The dual mode built-in self-test controller of claim 13, wherein the memory
2 executing means comprises:

- 3 a plurality of alternative memory built-in self-test state machines; and
4 a nested memory built-in self-test engine operating a predetermined one of the
5 memory built-in self-test state machines.

1 18. An integrated circuit device, comprising:

- 2 a plurality of memory components;
3 a logic core;
4 a testing interface; and
5 a dual mode built-in self-test controller controlled through the testing interface,
6 comprising:
7 a logic built-in self-test domain, including:
8 a logic built-in self-test engine capable of executing a logic built-in
9 self-test on the logic core; and
10 a logic built-in self-test signature generated by an execution of the
11 logic built-in self-test; and
12 a memory built-in self-test domain, including:
13 a memory built-in self-test engine capable of executing a memory
14 built-in self-test on the memory components.

1 19. The integrated circuit device of claim 18, wherein the logic built-in self-test
2 engine comprises:

- 3 a logic built-in self-test state machine; and
4 a pattern generator capable of generating a scan pattern for use in a state of the logic
5 built-in self-test state machine.

1 20. The integrated circuit device of claim 18, wherein the memory built-in self-
2 test domain further comprises a memory built-in self-test signature register generated by an
3 execution of the memory built-in self-test.

1 21. The integrated circuit device of claim 18, wherein the memory built-in self-
2 test engine comprises:
3 a memory built-in self-test state machine; and
4 a nested memory built-in self-test engine operating the memory built-in self-test state
5 machine.

1 22. The integrated circuit device of claim 18, wherein the memory built-in self-
2 test engine comprises:
3 a plurality of alternative memory built-in self-test state machines; and
4 a nested memory built-in self-test engine operating a predetermined one of the
5 memory built-in self-test state machines.

1 23. The integrated circuit device of claim 18, wherein the memory components
2 include a static random access memory device.

1 24. The integrated circuit device of claim 18, wherein testing interface comprises
2 a Joint Test Action Group tap controller.

1 25. A method for performing a built-in self-test on an integrated circuit device,
2 comprising:
3 externally resetting a dual mode built-in self-test controller;
4 performing at least one of a logic built-in self-test and a memory built-in self-test
5 from the dual mode built-in self-test controller; and
6 obtaining the results of the performed built-in self-test.

1 26. The method of claim 25, wherein externally resetting the dual mode built-in
2 self-test controller includes at least one of resetting a logic built-in self-test state machine in a
3 logic built-in self-test engine and resetting a memory built-in self-test state machine in a
4 memory built-in self-test engine.

1 27. The method of claim 25, wherein resetting the dual mode built-in self-test
2 controller includes initializing a multiple input signature register and a pattern generator in a
3 logic built-in self-test domain of the dual mode built-in self-test controller.

1 28. The method of claim 25, wherein performing the logic built-in self-test
2 includes:

3 initiating a plurality of components and signals in a logic built-in self-test domain of
4 the dual mode built-in self-test controller upon receipt of a logic built-in self-
5 test run signal;

6 scanning a scan chain upon the initialization of the components and the signals;

7 stepping to a new scan chain; and

8 repeating the previous scanning and stepping until the content of a pattern generator
9 equals a predetermined vector count.

10 29. The method of claim 28, further comprising at least one of:

11 setting a bit in the multiple input signature register indicating an error condition arose;
12 and

13 setting a bit in the multiple input signature register indicating whether the stored
14 results are from a previous logic built-in self-test run.

15 30. The method of claim 25, wherein performing the memory built-in self-test
16 includes:

17 initiating a plurality of components and signals in a memory built-in self-test domain
18 of the dual mode built-in self-test controller upon receipt of at least one of a
19 memory built-in self-test run signal and a memory built-in self-test select
20 signal;

21 flushing the contents of a plurality of memory components to a known state after
22 initialization of the components and the signals in the memory built-in self-test
23 domain; and

24 testing the flushed memory components.

25 31. The method of claim 30, wherein performing the memory built-in self-test
26 further includes at least one of:

27 storing the results of the memory built-in self-test in a memory built-in self-test
28 signature register;

5 storing the results of at least one paranoid check in the memory built-in self-test
6 signature register;
7 setting a bit in the memory built-in self-test signature register indicating whether the
8 memory built-in self-test is done.

1 32. A method for testing an integrated circuit device, comprising:
2 interfacing the integrated circuit device with a tester;
3 externally resetting a dual mode built-in self-test controller;
4 performing a logic built-in self-test from the dual mode built-in self-test controller;
5 performing a memory built-in self-test from the dual mode built-in self-test controller;
6 obtaining the results of the performed logic built-in self-test and the performed
7 memory built-in self-test.

33. The method of claim 32, wherein externally resetting the dual mode built-in
self-test controller includes at least one of resetting a logic built-in self-test state machine in a
logic built-in self-test engine and resetting a memory built-in self-test state machine in a
memory built-in self-test engine.

34. The method of claim 32, wherein performing the logic built-in self-test
includes:

initiating a plurality of components and signals in a logic built-in self-test domain of
the dual mode built-in self-test controller upon receipt of a logic built-in self-
test run signal;
scanning a scan chain upon the initialization of the components and the signals;
stepping to a new scan chain; and
repeating the previous scanning and stepping until the content of a pattern generator
equals a predetermined vector count.

35. The method of claim 32, wherein performing the memory built-in self-test
includes:

initiating a plurality of components and signals in a memory built-in self-test domain
of the dual mode built-in self-test controller upon receipt of at least one of a
memory built-in self-test run signal and a memory built-in self-test select
signal;

7 flushing the contents of a plurality of memory components to a known state after
8 initialization of the components and the signals in the memory built-in self-test
9 domain; and
10 testing the flushed memory components.

1 36. The method of claim 32, wherein obtaining the results includes reading at least
2 one of a logic built-in self-test signature and a memory built-in self-test signature.

1 37. The method of claim 32, wherein interfacing the integrated circuit device with
2 the tester includes employing Joint Test Action Group protocols.

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